AK

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/287,190	04/06/1999	MASAAKI ASANO	DAIN:496	5998

7590 08/08/2003

PARKHURST & WENDEL LLP
1421 PRINCE STREET
SUITE 210
ALEXANDRIA, VA 223142805

EXAMINER	
BERCK, KENNETH A	

ART UNIT	PAPER NUMBER
2879	

DATE MAILED: 08/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	09/287,190	ASANO ET AL.	
	Examiner	Art Unit	
	Ken A Berck	2879	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Amendment D, filed May 16, 2003, has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 and 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sano et al. (US 6249264) in view of Anderson et al. (US 6448946).

Regarding claim 1, Sano discloses a plasma display panel (fig 4) with a front plate (11) and a back plate (21) parallel to and facing each other having a space therebetween for a discharge gas, plural pairs of display electrodes (EP) on the front plate parallel to each other, with each display electrode pair comprising a sustain electrode (41) and a bus electrode (42), a dielectric layer (17) covering the display electrodes, and a protective film (18), address electrodes (22) on the back plate at right angles to the display electrode pairs, linear ribs (29) located between the address electrodes, with phosphor layers (28) located on the back plate between adjacent linear ribs so that the phosphor layers each extend intermittently in the lengthwise direction of the ribs for each pixel, the phosphor layers cover both the electrode and the linear ribs within each pixel, each pixel is formed by a crossing region of the address electrode and the display electrode pair, and each phosphor extends intermittently in the lengthwise

direction of the ribs so that the phosphor layer does not exist in the region on the ribs that corresponds to the region between the adjacent display electrode pairs.

Sano fails to clearly point out a dielectric layer on the bottom substrate covering the electrode.

Anderson discloses a dielectric layer on the bottom substrate covering the electrode in order to protect the electrode structure from the discharge and prevent further damage of the electrode structure.

Hence it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the display of Sano with the dielectric layer on the bottom substrate covering the electrode in order to protect the electrode structure from the discharge and prevent further damage of the electrode structure, as taught by Anderson.

Regarding claim 2, Sano discloses (7a) linear shield layers (50) on the front plate parallel to each other, with each layer located between an adjacent display electrode pair to be parallel to the display electrode pairs.

Regarding claim 3, Sano discloses a plasma display panel (fig 4) with a front plate (11) and a back plate (21) parallel to and facing each other having a space therebetween for a discharge gas, plural pairs of display electrodes (EP) on the front plate parallel to each other, with each display electrode pair comprising a sustain electrode (41) and a bus electrode (42), a dielectric layer (17) covering the display electrodes, and a protective film (18), address electrodes (22) on the back plate at right angles to the display electrode pairs, linear ribs (29) located between the address

electrodes, with phosphor layers (28) located on the back plate between adjacent linear ribs so that the phosphor layers each extend intermittently in the lengthwise direction of the ribs for each pixel, the phosphor layers cover both the electrode and the linear ribs within each pixel, each pixel is formed by a crossing region of the address electrode and the display electrode pair, and each phosphor extends intermittently in the lengthwise direction of the ribs so that the phosphor layer does not exist in the region on the ribs that corresponds to the region between the adjacent display electrode pairs.

Sano fails to clearly point out a dielectric layer on the bottom substrate covering the electrode.

Anderson discloses a dielectric layer on the bottom substrate covering the electrode in order to protect the electrode structure from the discharge and prevent further damage of the electrode structure.

Hence it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the display of Sano with the dielectric layer on the bottom substrate covering the electrode in order to protect the electrode structure from the discharge and prevent further damage of the electrode structure, as taught by Anderson.

Regarding claim 9, Sano discloses a plasma display panel (fig 4) with a front plate (11) and a back plate (21) parallel to and facing each other having a space therebetween for a discharge gas, plural pairs of display electrodes (EP) on the front plate parallel to each other, with each display electrode pair comprising a sustain electrode (41) and a bus electrode (42), a dielectric layer (17) covering the display

electrodes, and a protective film (18), address electrodes (22) on the back plate at right angles to the display electrode pairs, linear ribs (29) located between the address electrodes, with phosphor layers (28) located on the back plate between adjacent linear ribs so that the phosphor layers each extend intermittently in the lengthwise direction of the ribs for each pixel, the phosphor layers cover both the electrode and the linear ribs within each pixel, each pixel is formed by a crossing region of the address electrode and the display electrode pair, and each phosphor extends intermittently in the lengthwise direction of the ribs so that the phosphor layer does not exist in the region on the ribs that corresponds to the region between the adjacent display electrode pairs.

Sano fails to clearly point out a dielectric layer on the bottom substrate covering the electrode.

Anderson discloses a dielectric layer on the bottom substrate covering the electrode in order to protect the electrode structure from the discharge and prevent further damage of the electrode structure.

Hence it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the display of Sano with the dielectric layer on the bottom substrate covering the electrode in order to protect the electrode structure from the discharge and prevent further damage of the electrode structure, as taught by Anderson.

Regarding claim 10, Sano discloses (7a) linear shield layers (50) on the front plate parallel to each other, with each layer located between an adjacent display electrode pair to be parallel to the display electrode pairs.

Claims 4-8 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sano et al. (US 6249264) in view of Anderson et al. (US 6448946) and Mizobata (US 6333600).

Regarding claim 4, Sano and Anderson discloses all of the above claim limitations but fail to clearly point out the light-absorbing layer contains a dark pigment.

Mizobata discloses (fig 2) a light-absorbing layer (13) contains a dark pigment and a dielectric in order to achieve controlled reflectance and higher contrast.

Hence it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the display of Sano with the dielectric layer on the bottom substrate covering the electrode in order to excite the gas contained between the substrates and produce a glow discharge, as taught by Anderson, and a light-absorbing layer (13) contains a dark pigment and a dielectric in order to achieve controlled reflectance and higher contrast, as taught by Mizobata.

Regarding claim 5, Sano discloses a plasma display panel (fig 4) with a front plate (11) and a back plate (21) parallel to and facing each other having a space therebetween for a discharge gas, plural pairs of display electrodes (EP) on the front plate parallel to each other, with each display electrode pair comprising a transparent sustain electrode (41) and a metal bus electrode (42), a dielectric layer (17) covering the display electrodes, and a protective film (18) of MgO, address electrodes (22) on the back plate at right angles to the display electrode pairs, linear ribs (29) located between the address electrodes, with phosphor layers (28) located on the back plate between adjacent linear ribs so that the phosphor layers each extend intermittently in the

lengthwise direction of the ribs for each pixel, the phosphor layers cover both the electrode and the linear ribs within each pixel, each pixel is formed by a crossing region of the address electrode and the display electrode pair, and each phosphor extends intermittently in the lengthwise direction of the ribs so that the phosphor layer does not exist in the region on the ribs that corresponds to the region between the adjacent display electrode pairs.

Sano fails to clearly point out a dielectric layer on the bottom substrate covering the electrode with a dark dielectric.

Anderson discloses a dielectric layer on the bottom substrate covering the electrode in order to protect the electrode structure from the discharge and prevent further damage of the electrode structure but fails to clearly point out a dark dielectric.

Mizobata discloses (fig 2) a light-absorbing layer (13) contains a dark pigment and a dielectric in order to achieve controlled reflectance and higher contrast.

Hence it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the display of Sano with the dielectric layer on the bottom substrate covering the electrode in order to protect the electrode structure from the discharge and prevent further damage of the electrode structure, as taught by Anderson, and a light-absorbing layer (13) contains a dark pigment and a dielectric in order to achieve controlled reflectance and higher contrast, as taught by Mizobata.

Regarding claim 6, Sano discloses (7a) linear shield layers (50) on the front plate parallel to each other, with each layer located between an adjacent display electrode pair to be parallel to the display electrode pairs.

Regarding claims 7-8 and 11, Sano discloses a plasma display panel (fig 4) with a front plate (11) and a back plate (21) parallel to and facing each other having a space therebetween for a discharge gas, plural pairs of display electrodes (EP) on the front plate parallel to each other, with each display electrode pair comprising a transparent sustain electrode (41) and a metal bus electrode (42), a dielectric layer (17) covering the display electrodes, and a protective film (18) of MgO, address electrodes (22) on the back plate at right angles to the display electrode pairs, linear ribs (29) located between the address electrodes, with phosphor layers (28) located on the back plate between adjacent linear ribs so that the phosphor layers each extend intermittently in the lengthwise direction of the ribs for each pixel, the phosphor layers cover both the electrode and the linear ribs within each pixel, each pixel is formed by a crossing region of the address electrode and the display electrode pair, and each phosphor extends intermittently in the lengthwise direction of the ribs so that the phosphor layer does not exist in the region on the ribs that corresponds to the region between the adjacent display electrode pairs.

Sano fails to clearly point out a dielectric layer on the bottom substrate covering the electrode with a dark dielectric.

Anderson discloses a dielectric layer on the bottom substrate covering the electrode in order to protect the electrode structure from the discharge and prevent further damage of the electrode structure but fails to clearly point out a dark dielectric.

Mizobata discloses (fig 2) a light-absorbing layer (13) contains a dark pigment and a dielectric in order to achieve controlled reflectance and higher contrast.

Hence it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the display of Sano with the dielectric layer on the bottom substrate covering the electrode in order to protect the electrode structure from the discharge and prevent further damage of the electrode structure, as taught by Anderson, and a light-absorbing layer (13) contains a dark pigment and a dielectric in order to achieve controlled reflectance and higher contrast, as taught by Mizobata.

Contact information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ken A Berck whose telephone number is (703)305-7984. The examiner can normally be reached on Mon-Fri 8:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimesh Patel can be reached on (703)305-4794. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7382 for regular communications and (703)308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

kab
July 28, 2003

Joseph Williams